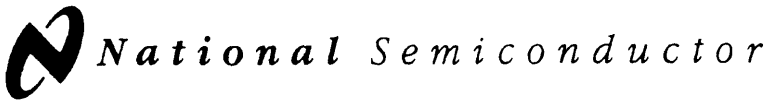


395-328

NM93C06/C46/C56/C66



NM93C06/C46/C56/C66 256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

General Description

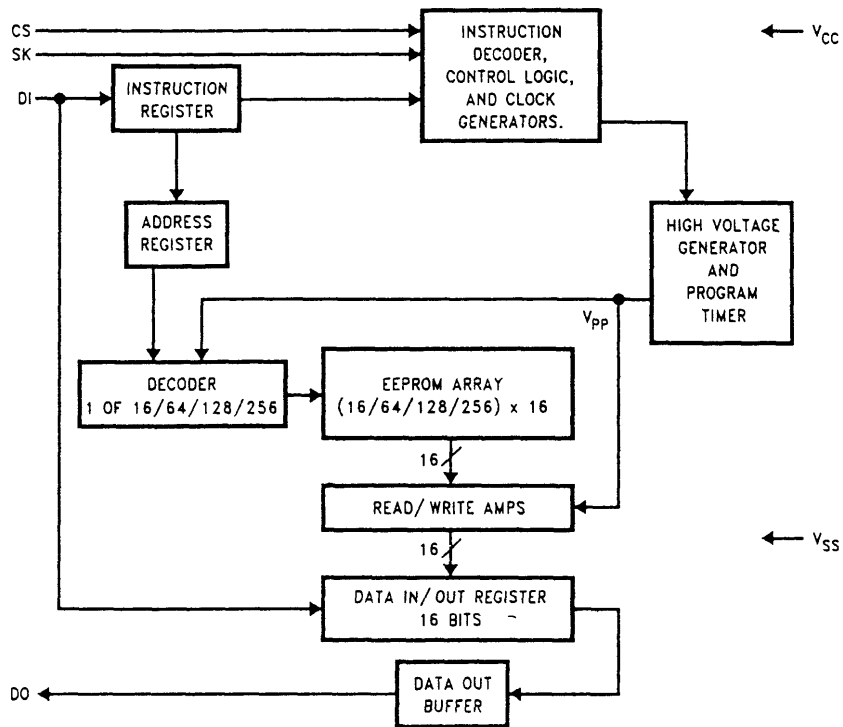
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in both SO and TSSOP packages for small space considerations.

The EEPROM Interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- Device status during programming mode
- Typical active current of 200 μ A; Typical standby current of 10 μ A
- No erase required before write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

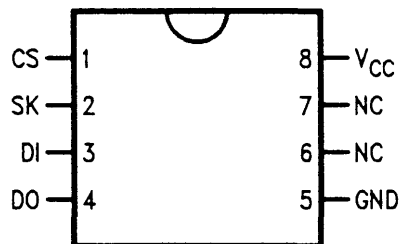
Block Diagram



TL/D/10751-1

Connection Diagrams

Dual-In-Line Package (N)
8-Pin SO (M8) and 8-Pin TSSOP (MT8)



Top View

See NS Package Number
N08E, M08A and MTC08

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Pin Names

| | |
|-----------------|--------------------|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| V _{CC} | Power Supply |

Ordering Information

Commercial Temp. Range (0°C to +70°C)

| Order Number |
|-----------------------|
| NM93C06N/NM93C46N |
| NM93C56N/NM93C66N |
| NM93C06M8/NM93C46M8 |
| NM93C56M8/NM93C66M8 |
| NM93C06MT8/NM93C46MT8 |
| NM93C56MT8/NM93C66MT8 |

Extended Temp. Range (-40°C to +85°C)

| Order Number |
|-------------------------|
| NM93C06EN/NM93C46EN |
| NM93C56EN/NM93C66EN |
| NM93C06EM8/NM93C46EM8 |
| NM93C56EM8/NM93C66EM8 |
| NM93C06EMT8/NM93C46EMT8 |
| NM93C56EMT8/NM93C66EMT8 |

Automotive Temp. Range (-40°C to +125°C)

| Order Number |
|-------------------------|
| NM93C06VN/NM93C46VN |
| NM93C56VN/NM93C66VN |
| NM93C06VM8/NM93C46VM8 |
| NM93C56VM8/NM93C66VM8 |
| NM93C06VMT8/NM93C46VMT8 |
| NM93C56VMT8/NM93C66VMT8 |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-----------------|
| Ambient Storage Temperature | -65°C to +150°C |
| All Input or Output Voltages with Respect to Ground | +6.5V to -0.3V |
| Lead Temp. (Soldering, 10 sec.) | +300°C |
| ESD Rating | 2000V |

Operating Conditions

| | |
|---------------------------------|-----------------|
| Ambient Operating Temperature | 0°C to +70°C |
| NM93C06-NM93C66 | -40°C to +85°C |
| NM93C06E-NM93C66E | -40°C to +125°C |
| NM93C06V-NM93C66V | 4.5V to 5.5V |
| Power Supply (V _{CC}) | |

DC and AC Electrical Characteristics V_{CC} = 5.0V ± 10% unless otherwise specified

Note: Throughout this table, "M" refers to temperature range (-55°C to +125°C), not package.

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|--------------------------------------|---|--|---|-----------------------|----------------------------|----------|
| I _{CCA} | Operating Current | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | CS = V _{IH} , SK = 1 MHz SK = 1 MHz | | 1 1 | mA |
| I _{CCS} | Standby Current | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | CS = V _{IL} | | 50 50 | μA μA |
| I _{IL} I _{OL} | Input Leakage Output Leakage | | V _{IN} = 0V to V _{CC} (Note 3) | | ±1 | μA |
| V _{IL} V _{IH} | Input Low Voltage Input High Voltage | | | -0.1 2 | 0.8 V _{CC} + 1 | V |
| V _{OL1} V _{OH1} | Output Low Voltage Output High Voltage | | I _{OL} = 2.1 mA I _{OH} = -400 μA | 2.4 | 0.4 | V V |
| V _{OL2} V _{OH2} | Output Low Voltage Output High Voltage | | I _{OL} = 10 μA I _{OH} = -10 μA | V _{CC} - 0.2 | 0.2 | V |
| f _{SK} | SK Clock Frequency | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | (Note 4) | 0 0 | 1 1 | MHz |
| t _{SKH} | SK High Time | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | | 250 300 | | ns |
| t _{SKL} | SK Low Time | | | 250 | | ns |
| t _{SKS} | SK Setup Time | | SK must be at V _{IL} for t _{SKS} before CS goes high | 50 | | ns |
| t _{CS} | Minimum CS Low Time | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | (Note 2) | 250 250 | | ns |

DC and AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$ (unless otherwise specified) (Continued)

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|-----------|------------------------|--|---------------|------------|------------|-------|
| t_{CSS} | CS Setup Time | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | | 50 50 | | ns |
| t_{DH} | DO Hold Time | | | 70 | | ns |
| t_{DIS} | DI Setup Time | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | | 100 200 | | ns |
| t_{CSH} | CS Hold Time | | | 0 | | ns |
| t_{DIH} | DI Hold Time | | | 20 | | ns |
| t_{PD1} | Output Delay to "1" | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | | | 500 500 | ns |
| t_{PD0} | Output Delay to "0" | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | | | 500 500 | ns |
| t_{SV} | CS to Status Valid | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | | | 500 500 | ns |
| t_{DF} | CS to DO in TRI-STATE® | NM93C06-NM93C66 NM93C06E/V-NM93C66E/V | CS = V_{IL} | | 100 100 | ns |
| t_{WP} | Write Cycle Time | | | | 10 | ms |

Capacitance

$T_A = 25^\circ C$ $f = 1$ MHz

| Symbol | Test | Typ | Max | Units |
|-----------|--------------------|-----|-----|-------|
| C_{OUT} | Output Capacitance | | 5 | pF |
| C_{IN} | Input Capacitance | | 5 | pF |

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams in the following pages).

Note 3: Typical leakage values are in the 20 nA range.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\text{minimum}} + t_{SKL\text{minimum}}$ for shorter SK cycle time operation.

AC Test Conditions

| V_{CC} Range | V_{IL}/V_{IH} Input Levels | V_{IL}/V_{IH} Timing Level | V_{OL}/V_{OH} Timing Level | I_{OL}/I_{OH} |
|--|---------------------------------|---------------------------------|---------------------------------|-----------------|
| $4.5V \leq V_{CC} \leq 5.5V$ (TTL Levels) | 0.4V/2.4V | 1.0V/2.0V | 0.4V/2.4V | -2.1 mA/0.4 mA |

Output Load: 1 TTL Gate ($C_L = 100$ pF)

Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

All Data in signals are clocked into the device on the low-to-high SK transition.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical '0' indicates that programming is still in progress. DO = logical

NOTE: The NSC CMOS EEPROMs do not require an 'ERASE' or 'ERASE ALL' operation prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06 and NM93C46

| Instruction | SB | Op Code | Address | Data | Comments |
|-------------|----|---------|---------|--------|--|
| READ | 1 | 10 | A5-A0 | | Reads data stored in memory, at specified address. |
| WEN | 1 | 00 | 11XXXX | | Enable all programming modes. |
| ERASE | 1 | 11 | A5-A0 | | Erase selected register. |
| WRITE | 1 | 01 | A5-A0 | D15-D0 | Writes selected register. |
| ERAL | 1 | 00 | 10XXXX | | Erases all registers. |
| WRALL | 1 | 00 | 01XXXX | D15-D0 | Writes all registers. |
| WDS | 1 | 00 | 00XXXX | | Disables all programming modes. |

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06.

Instruction Set for the NM93C56 and NM93C66

| Instruction | SB | Op Code | Address | Data | Comments |
|-------------|----|---------|----------|--------|--|
| READ | 1 | 10 | A7-A0 | | Reads data stored in memory, at specified address. |
| WEN | 1 | 00 | 11XXXXXX | | Enable all programming modes. |
| ERASE | 1 | 11 | A7-A0 | | Erase selected register. |
| ERAL | 1 | 00 | 10XXXXXX | | Erases all registers. |
| WRITE | 1 | 01 | A7-A0 | D15-D0 | Writes selected register. |
| WRALL | 1 | 00 | 01XXXXXX | D15-D0 | Writes all registers. |
| WDS | 1 | 00 | 00XXXXXX | | Disables all programming modes. |

Note: Address bit A7 becomes "Don't Care" for the NM93C56

'1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

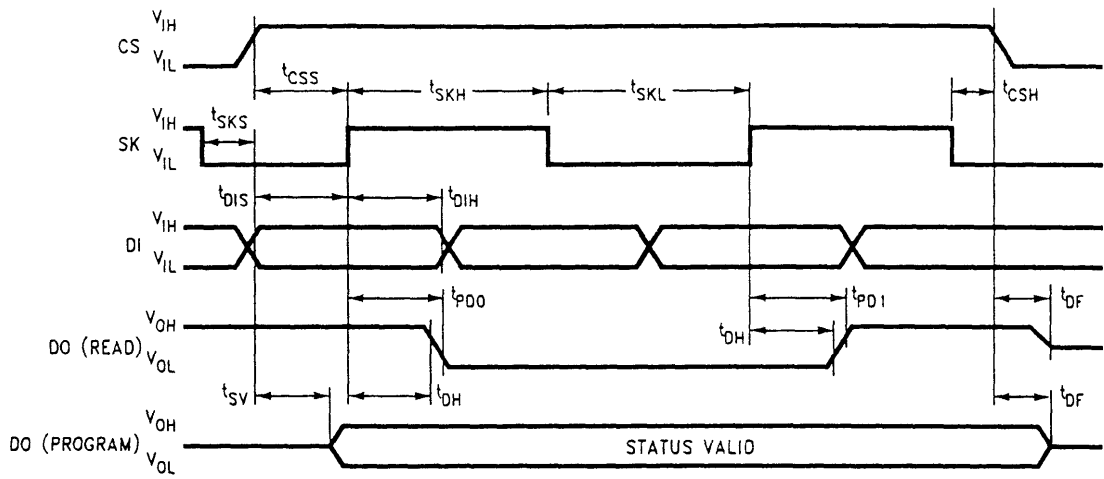
The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

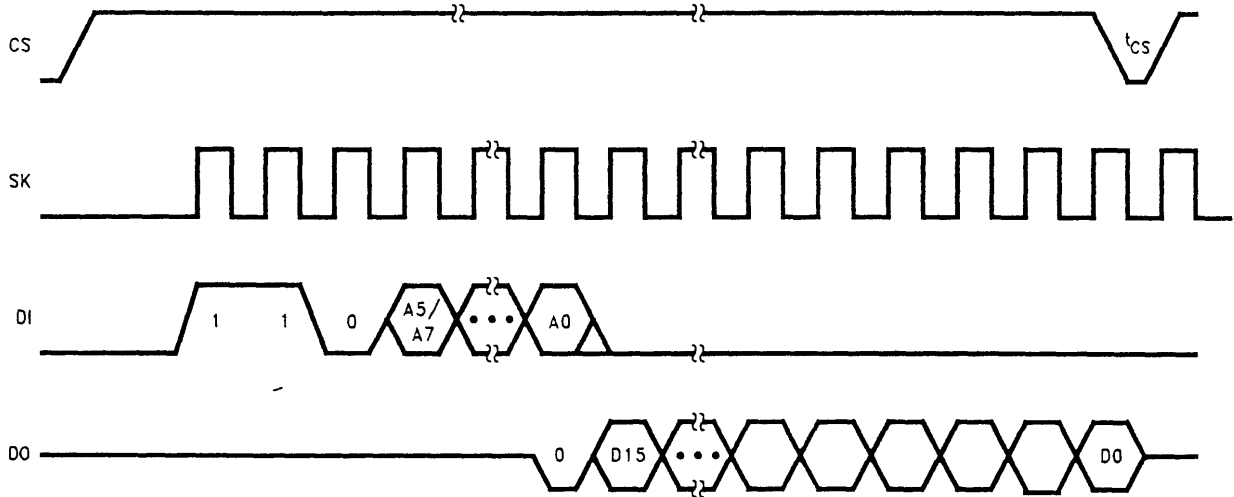
Timing Diagrams

Synchronous Data Timing



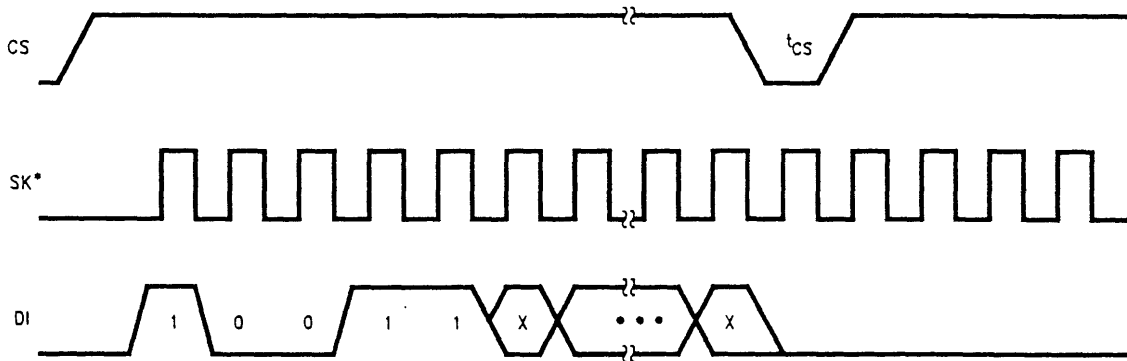
TL/D/10751-4

READ



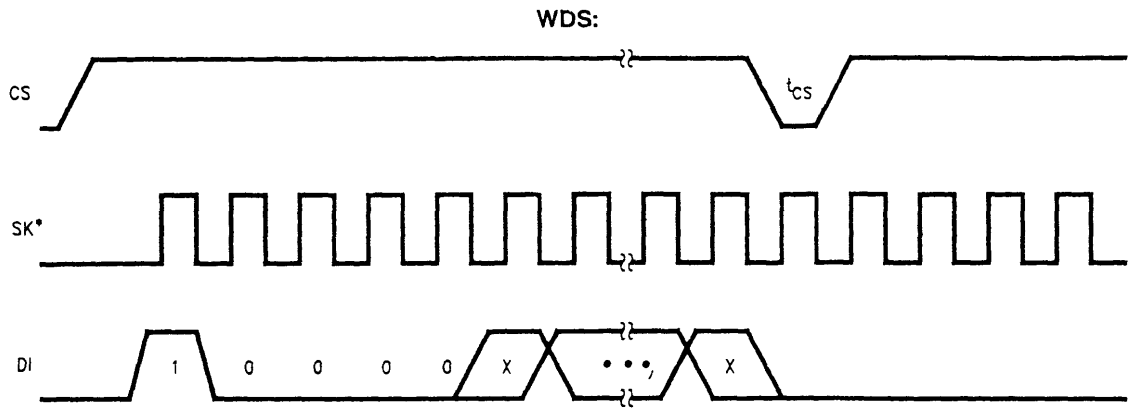
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WEN

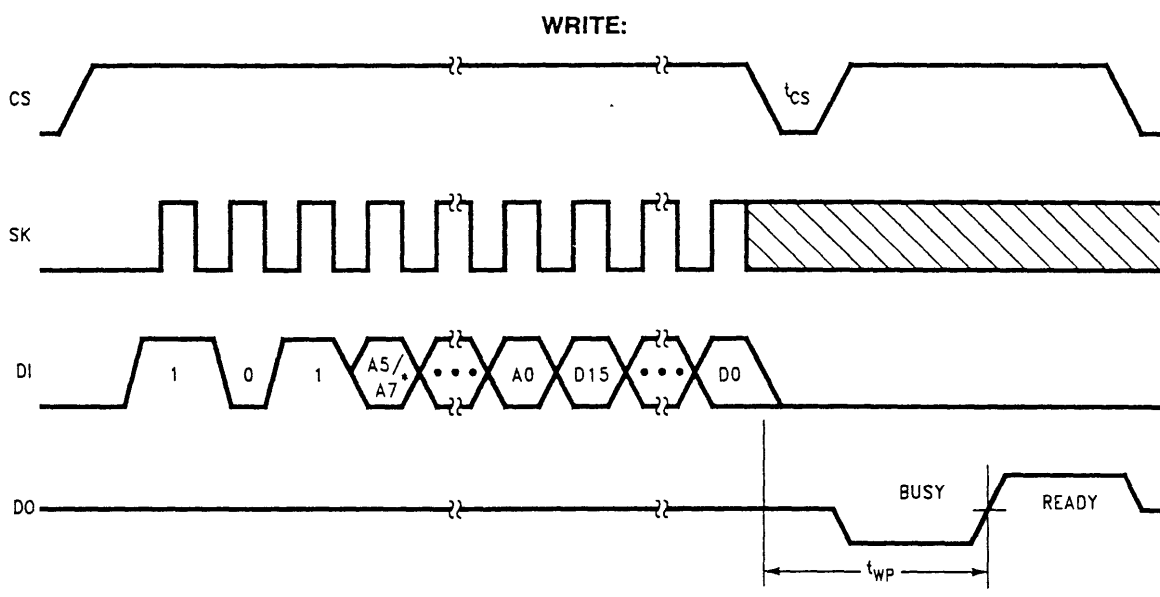


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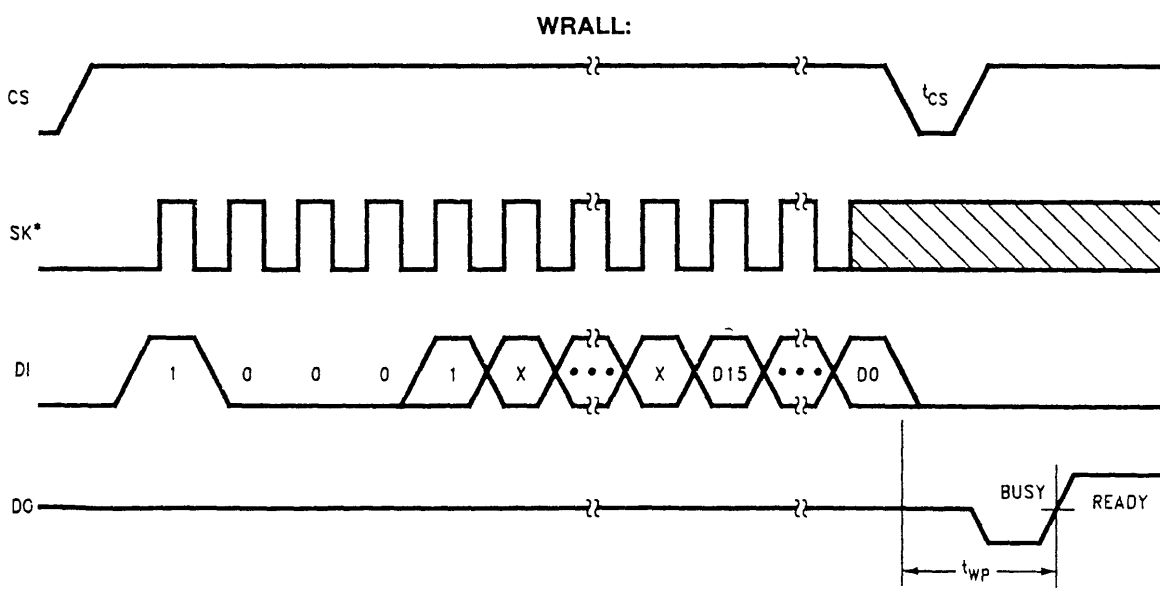
Timing Diagrams (Continued)



TL/D/10751-7



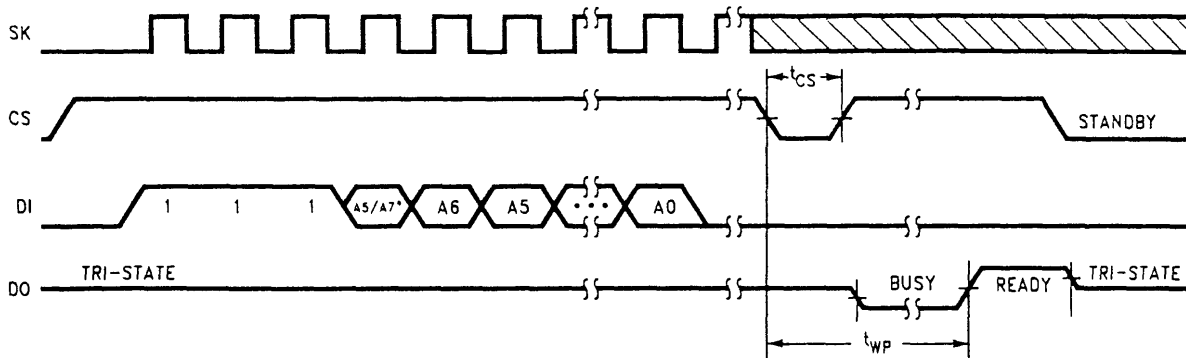
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TL/D/10751-9

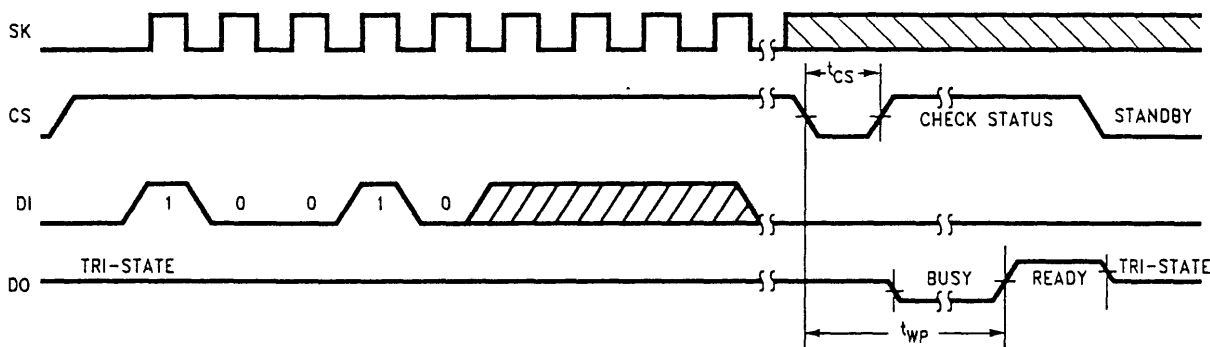
Timing Diagrams (Continued)

ERASE:



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ERAL:



TL/D/10751-11